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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/928,733	08/13/2001	Masaaki Nishijima	NAK1-BP73	7355

7590

12/13/2002

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EXAMINER

MANDALA, VICTOR A

ART UNIT

PAPER NUMBER

2826

DATE MAILED: 12/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/928,733

Applicant(s)

NISHIJIMA, MASAOKI

Examiner

Victor A Mandala Jr.

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 October 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 and 9-28 is/are pending in the application.
- 4a) Of the above claim(s) 1-6 and 10-26 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 7, 9, 27 and 28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Response to Applicant's Arguments

1. The Applicant amended the independent claims 7 and 9 to overcome the 35 U.S.C 112 2nd paragraph rejection and has also changed the scope of the invention. The 35 U.S.C 112 2nd paragraph rejection is withdrawn in light of Amendment B filed on 10/9/02, which also prompts the examiner to search the new scope of the invention. Claims 7, 9, 27, and 28 will be further examined.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7, 9, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted prior art in view of U.S. Patent No. 6,075,427 Tai et al.

2. Referring to claim 7, an RF passive circuit comprising: a semiconductor substrate, (Applicant's admitted prior art Figures 8A-8D #824 & Tai et al. Figure 4 #41); a via hole, (Applicant's admitted prior art Figures 8A-8D #821), through the semiconductor substrate,

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(Applicant's admitted prior art Figures 8A-8D #824 & Tai et al. Figure 4 #41), the via hole, (Applicant's admitted prior art Figures 8A-8D #821), having metal film, (Applicant's admitted prior art Figures 8A-8D #827), on an inside wall; a wiring metal layer, (Applicant's admitted prior art Figures 8A-8D #831 & Tai et al. Figure 4 #26), formed in a spiral pattern with an inside end on the semiconductor substrate, (Applicant's admitted prior art Figures 8A-8D #824 & Tai et al. Figure 4 #41), the wiring metal layer, (Applicant's admitted prior art Figures 8A-8D #831 & Tai et al. Figure 4 #26), being electrically connected, (Applicant's admitted prior art Page 5 Lines 11-14 & with the layer #828 being dielectric and between layer #831 and layer #829 it is apparent that there is an electrical contact with the via), to the via hole, (Applicant's admitted prior art Figures 8A-8D #821), at the inside end; an inductor of metal film, (Applicant's admitted prior art Figures 8A-8D #830 & Tai et al. Figure 4 #28), formed in a spiral pattern with an inside end on the wiring metal layer, (Applicant's admitted prior art Figures 8A-8D #831 & Tai et al. Figure 4 #26), with the inside end of the inductor film, (Applicant's admitted prior art Figures 8A-8D #830 & Tai et al. Figure 4 #28), being near the via hole, (Applicant's admitted prior art Figures 8A-8D #821); and a dielectric layer, (Applicant's admitted prior art Figures 8A-8D #828 & Tai et al. Figure 4 #44), between the spiral wiring metal layer, (Applicant's admitted prior art Figures 8A-8D #831 & Tai et al. Figure 4 #26), and the spiral inductor metal film, (Applicant's admitted prior art Figures 8A-8D #830 & Tai et al. Figure 4 #28).

The Applicant's prior art teaches all of the claimed matter in claim 7 except for the wiring metal layer being formed in a spiral shape, but Tai et al. does in Figure 4. It would have been obvious to one skilled in the art to combine the teachings of the Applicant's admitted prior art with the teachings of Tai et al. because designing an RF amplifier inductor with the highest

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possible quality factor, (Q), results in a more efficient MCM operation and the space requirements are greatly reduced, which is the direction of designs. Further information can be found in Tai et al., (Col. 3 Lines 19-26 & Col. 4 Lines 3-14).

3. Referring to claim 9, an RF choke used in at least one of a matching circuit, (Applicant's admitted prior art Figures 8A-8D #808), and a bias feeding circuit, (Applicant's admitted prior art Figures 8A-8D #807), both circuits being included in an RF amplifier, the RF choke comprising: a semiconductor substrate, (Applicant's admitted prior art Figures 8A-8D #824 & Tai et al. Figure 4 #41), where at least one of the matching circuit, (Applicant's admitted prior art Figures 8A-8D #808), and the bias feeding circuit, (Applicant's admitted prior art Figures 8A-8D #807), is incorporated; a via hole, (Applicant's admitted prior art Figures 8A-8D #821), through the semiconductor substrate, (Applicant's admitted prior art Figures 8A-8D #824 & Tai et al. Figure 4 #41), the via hole, (Applicant's admitted prior art Figures 8A-8D #821), having metal film, (Applicant's admitted prior art Figures 8A-8D #827), on an inside wall; a wiring metal layer, (Applicant's admitted prior art Figures 8A-8D #831 & Tai et al. Figure 4 #26), formed in a spiral pattern with an inside end on the semiconductor substrate, (Applicant's admitted prior art Figures 8A-8D #824 & Tai et al. Figure 4 #41), the wiring metal layer, (Applicant's admitted prior art Figures 8A-8D #831 & Tai et al. Figure 4 #26), being electrically connected, (Applicant's admitted prior art Page 5 Lines 11-14 & with the layer #828 being dielectric and between layer #831 and layer #829 it is apparent that there is an electrical contact with the via), to the via hole, (Applicant's admitted prior art Figures 8A-8D #821), at the inside end; an inductor of a metal film, (Applicant's admitted prior art Figures 8A-8D #830 & Tai et al. Figure 4 #28), formed in a spiral pattern with an inside end on the wiring metal layer, (Applicant's

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admitted prior art Figures 8A-8D #831 & Tai et al. Figure 4 #26), with the inside end of the inductor film, (Applicant's admitted prior art Figures 8A-8D #830 & Tai et al. Figure 4 #28), being near the via hole, (Applicant's admitted prior art Figures 8A-8D #821); and a dielectric layer, (Applicant's admitted prior art Figures 8A-8D #828 & Tai et al. Figure 4 #44), between the spiral wiring metal layer, (Applicant's admitted prior art Figures 8A-8D #831 & Tai et al. Figure 4 #26), and the spiral inductor metal film, (Applicant's admitted prior art Figures 8A-8D #830 & Tai et al. Figure 4 #28).

The Applicant's prior art teaches all of the claimed matter in claim 7 except for the wiring metal layer being formed in a spiral shape, but Tai et al. does in Figure 4. It would have been obvious to one skilled in the art to combine the teachings of the Applicant's admitted prior art with the teachings of Tai et al. because designing an RF amplifier inductor with the highest possible quality factor, (Q), results in a more efficient MCM operation and the space requirements are greatly reduced, which is the direction of designs. Further information can be found in Tai et al., (Col. 3 Lines 19-26 & Col. 4 Lines 3-14).

4. Referring to claim 27, an RF passive circuit, wherein the wiring metal layer is formed by an evaporation process, (Applicant's admitted prior art Page 4 Lines 23-24 & Page 5 Lines 1-2).

Initially, and with respect to claim 27, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hira, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

As to the grounds of rejection under section 103, see MPEP § 2113

5. Referring to claim 28, an RF passive circuit, wherein the inside end of the wiring metal layer, (Applicant's admitted prior art Figures 8A-8D #831 & Tai et al. Figure 4 #26), is connected to the via hole, (Applicant's admitted prior art Figures 8A-8D #821), by a ground layer, (Applicant's admitted prior art Figures 8A-8D #826), over one end of the via hole, (Applicant's admitted prior art Figures 8A-8D #821), on the semiconductor substrate, (Applicant's admitted prior art Figures 8A-8D #824 & Tai et al. Figure 4 #41).

The Applicant's prior art teaches all of the claimed matter in claim 7 except for the wiring metal layer being formed in a spiral shape, but Tai et al. does in Figure 4. It would have been obvious to one skilled in the art to combine the teachings of the Applicant's admitted prior art with the teachings of Tai et al. because designing an RF amplifier inductor with the highest possible quality factor, (Q), results in a more efficient MCM operation and the space requirements are greatly reduced, which is the direction of designs. Further information can be found in Tai et al., (Col. 3 Lines 19-26 & Col. 4 Lines 3-14).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

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will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ
December 2, 2002



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